

#4  
Formal  
drawings  
MHA  
3/4/02

Figure 1

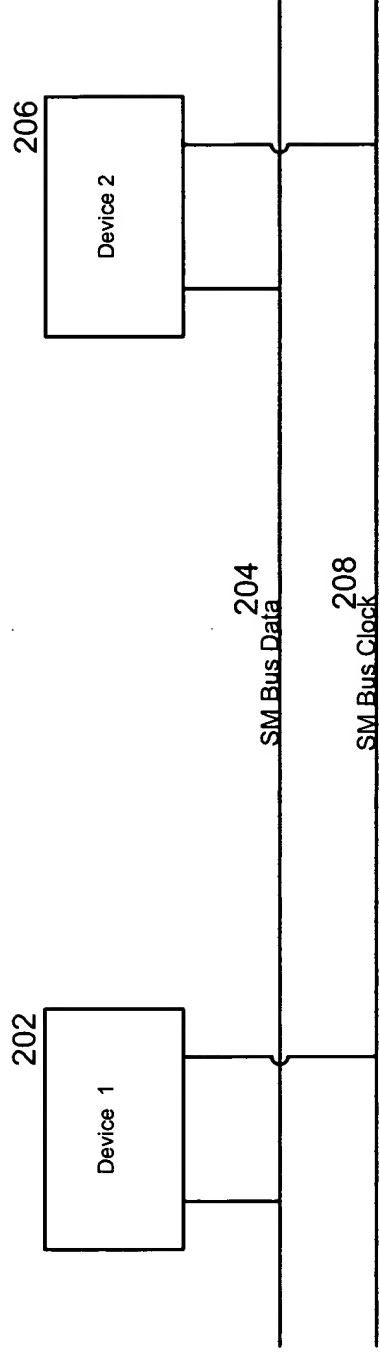


Figure 2

# Serial VID Interface

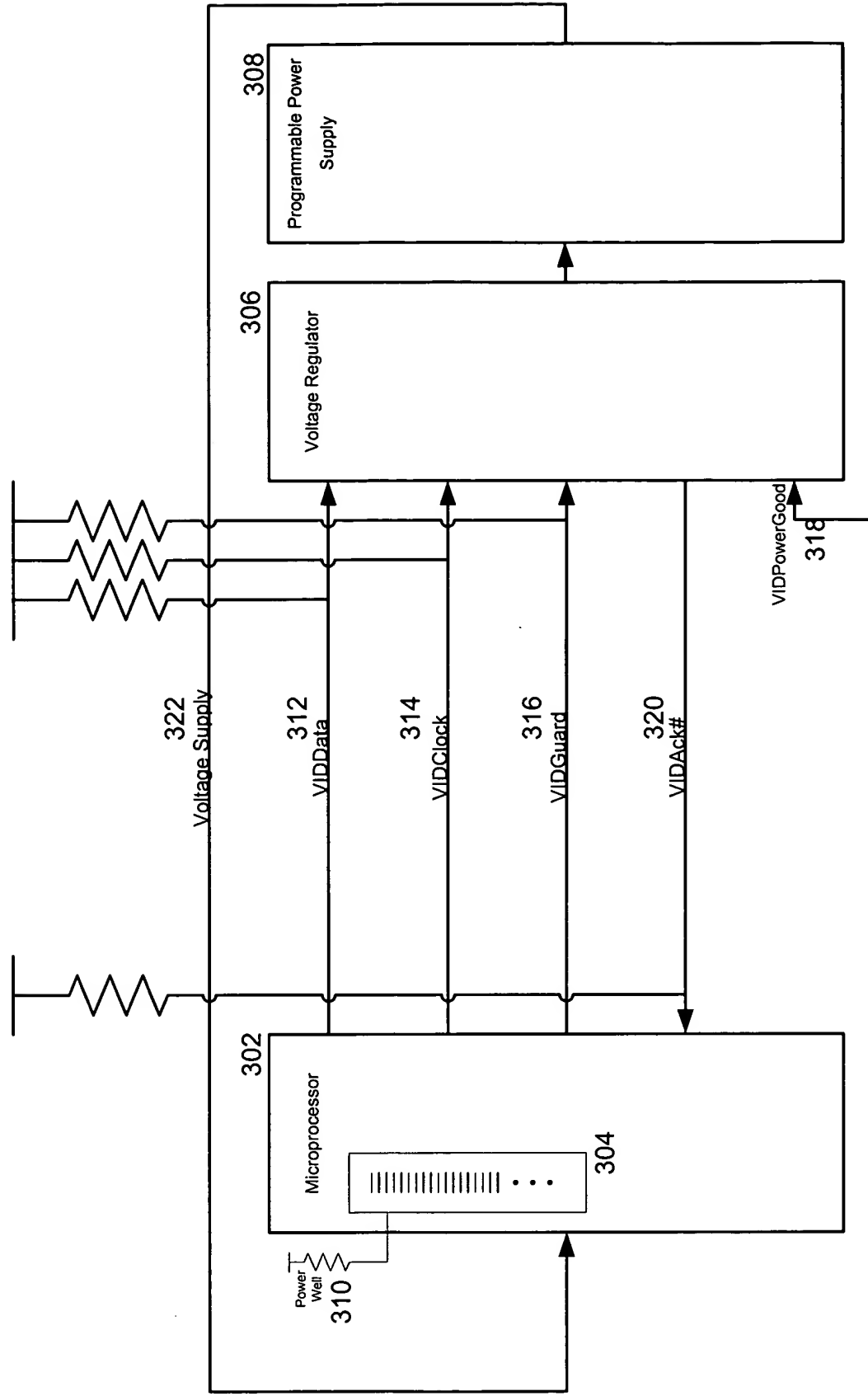


Figure 3

# VIDData and VIDGuard Timing

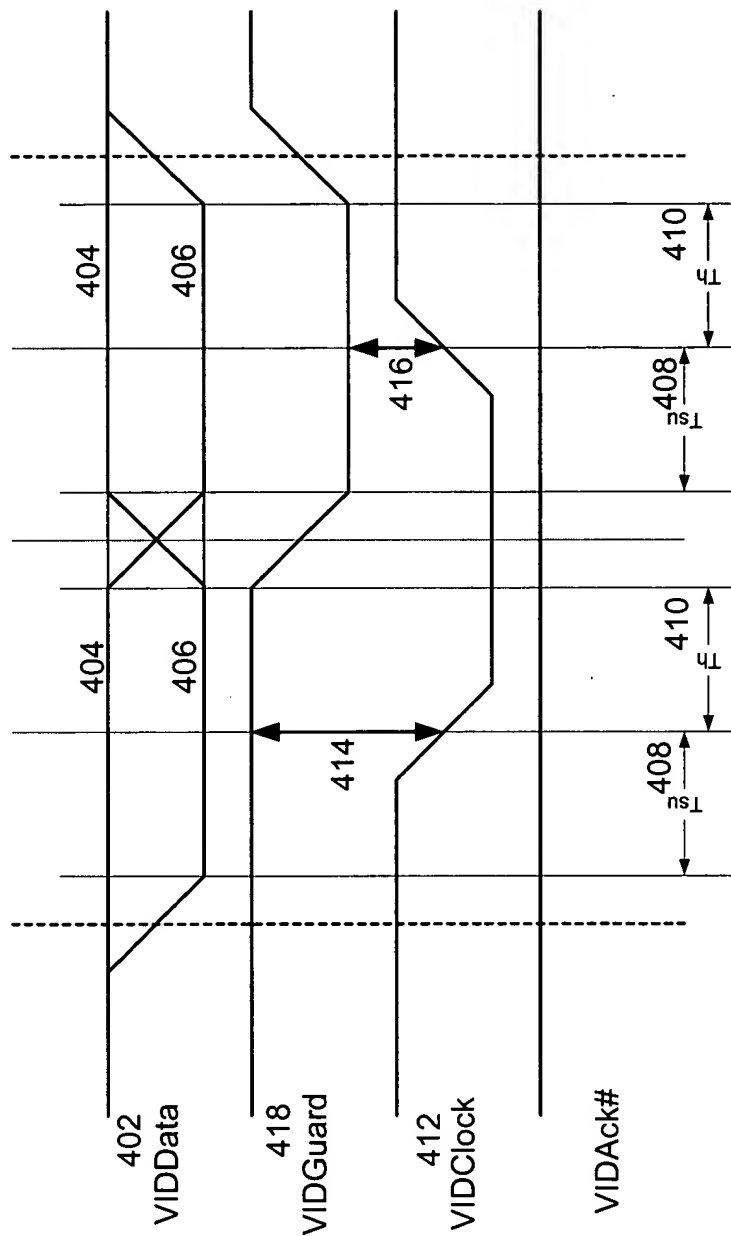


Figure 4

# VIDAck# Timing

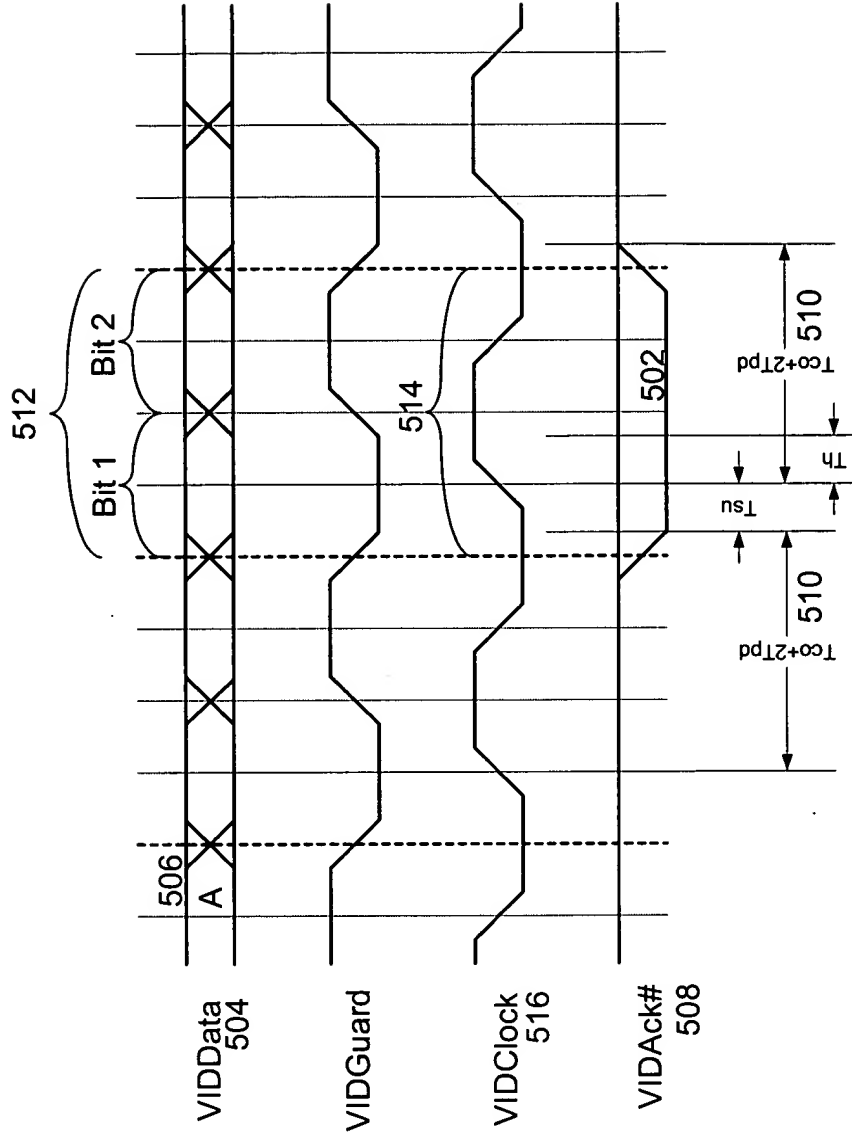


Figure 5

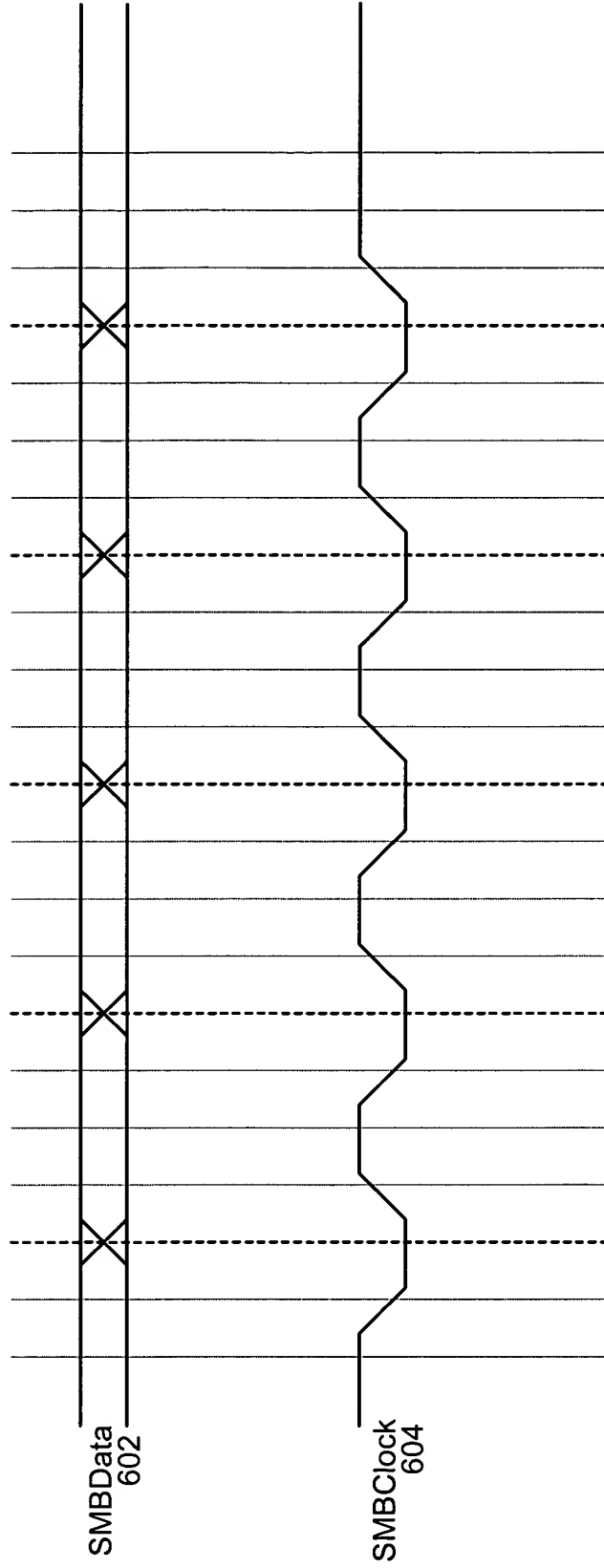


Figure 6

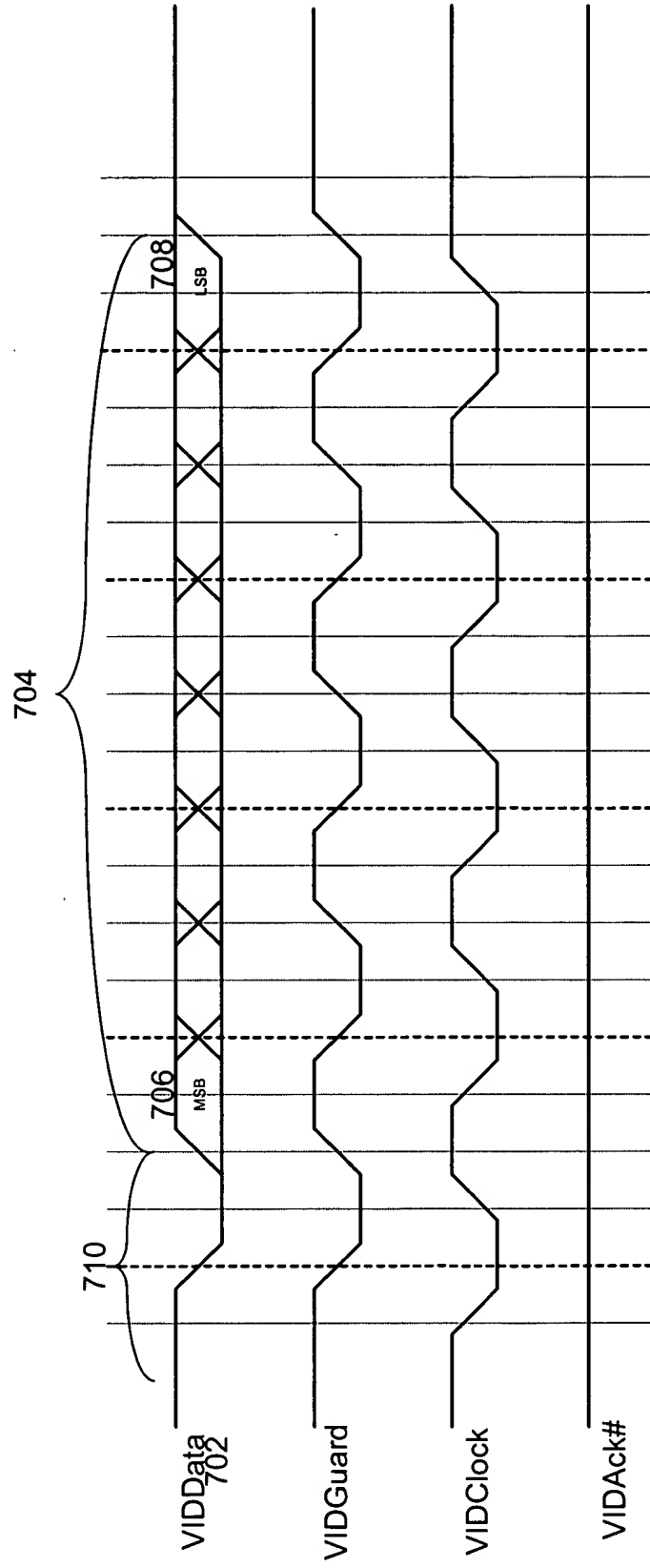


Figure 7

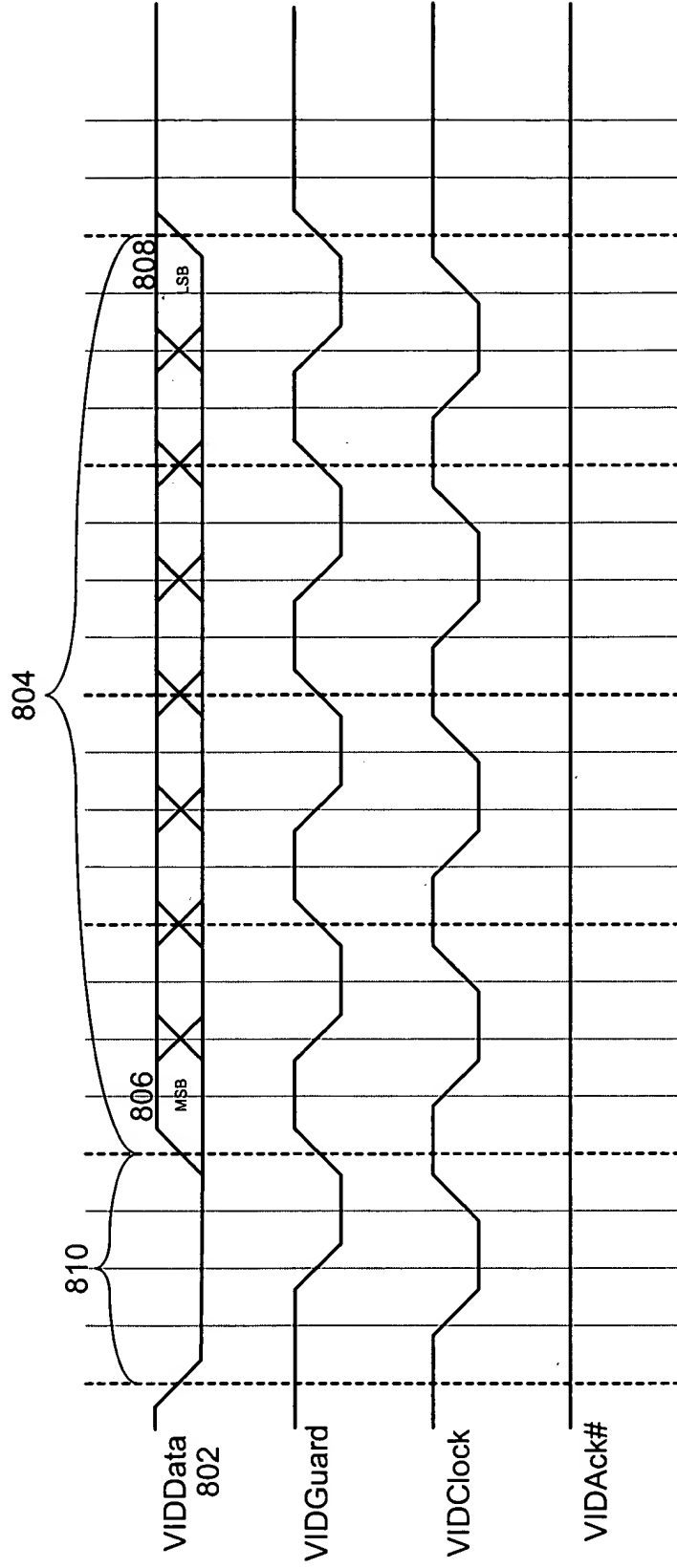


Figure 8

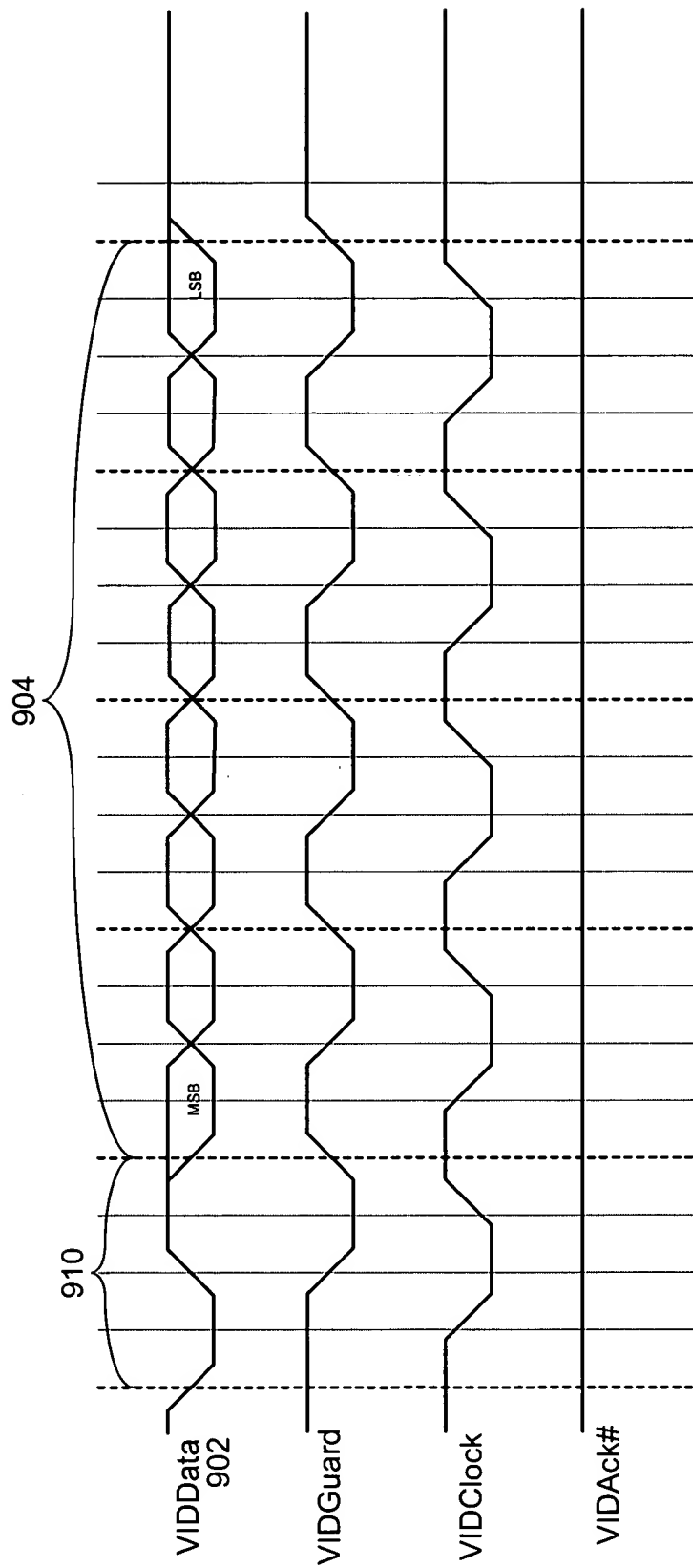


Figure 9

# Ack Byte with Positive Acknowledgement

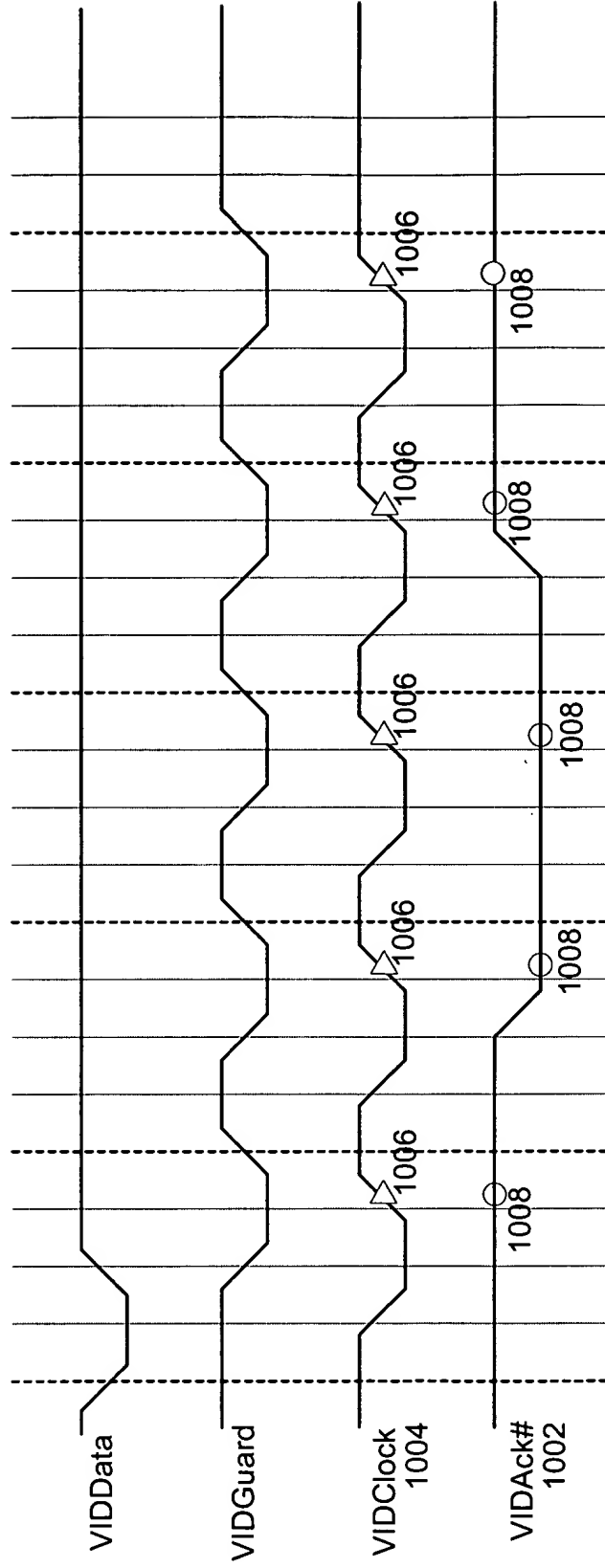


Figure 10

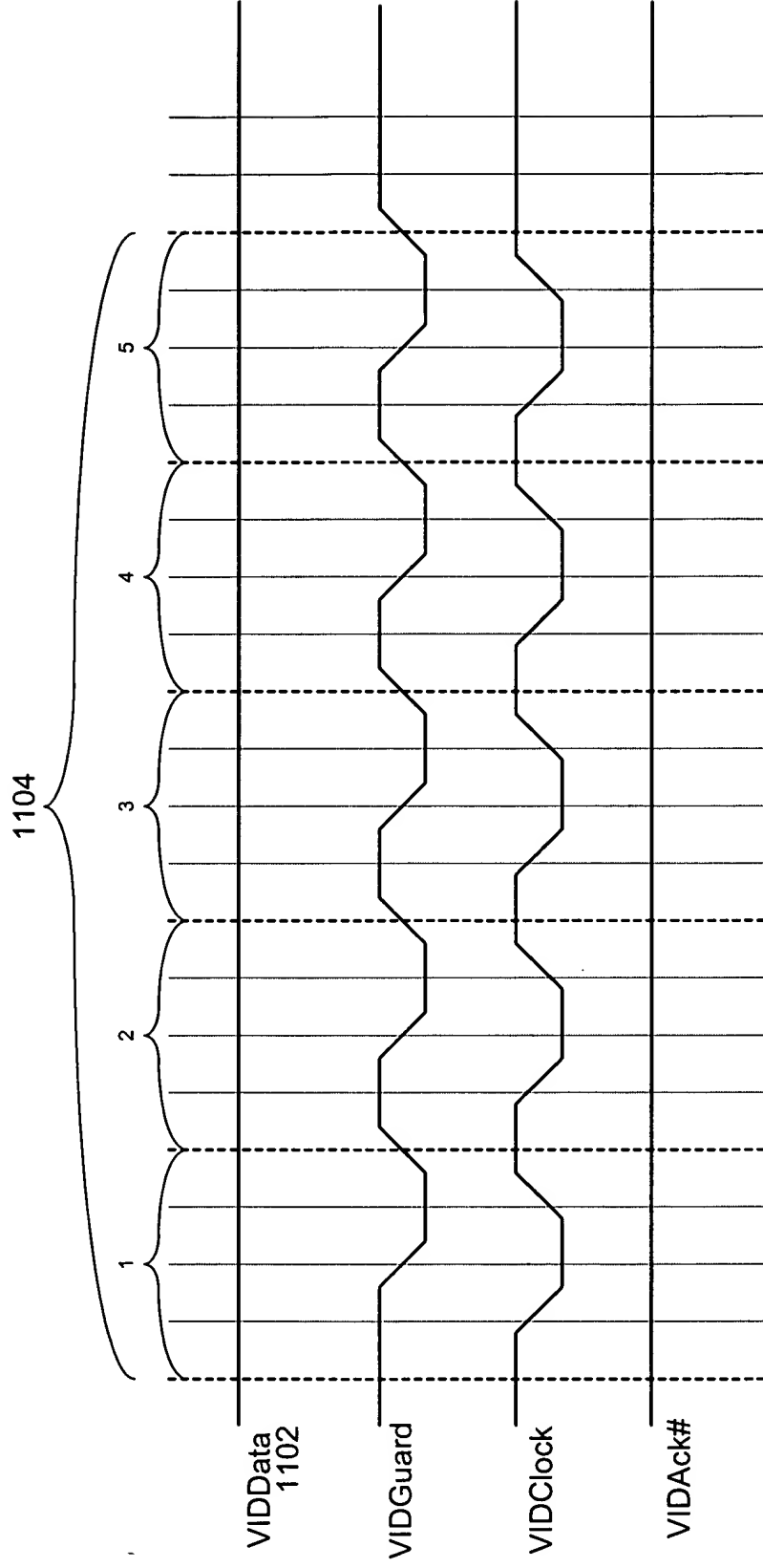


Figure 11

# Complete Command

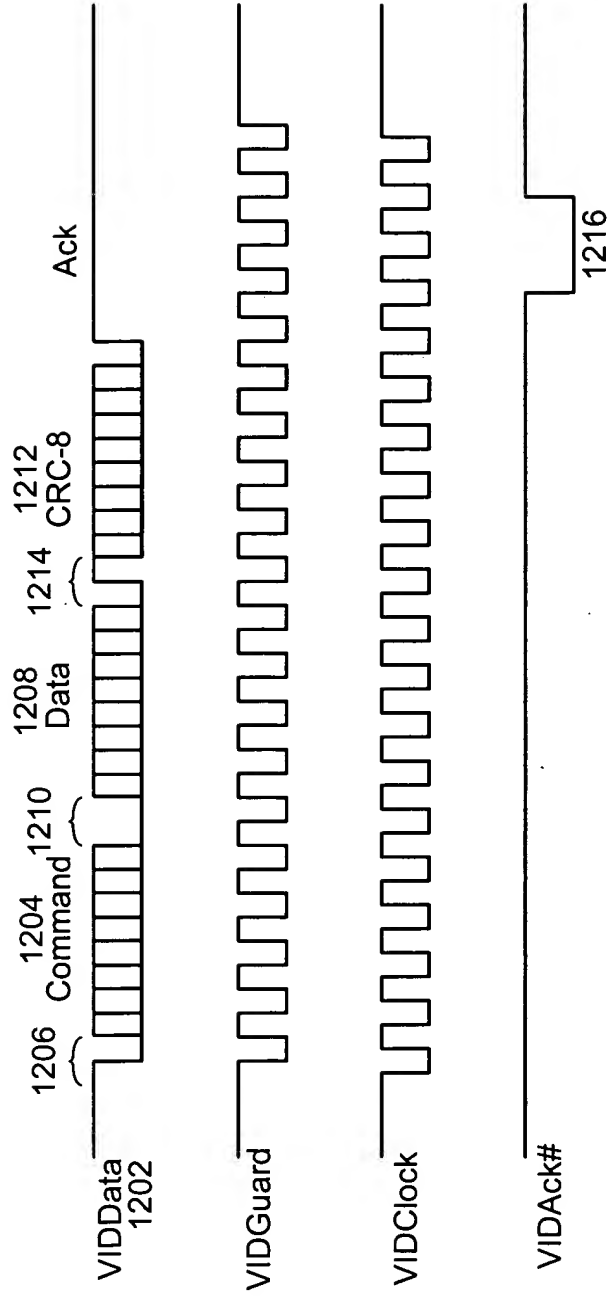


Figure 12